REMARKS

Claims 1-49 are cancelled. New claims 50 and 51 are added.

Claims 50 and 51 have been formulated to more clearly define the present invention and to define the invention over the prior art of record.

In particular, claim 50 recites a processing device comprising:

-a reconfigurable circuit including a plurality of data processing units,

-an internal state holding circuit for holding data being processed inside each of the data processing units,

-a memory portion for storing data provided from outputs of the data processing units, and

-a data processing unit of the plurality of the units includes multiple data processing sub-units.

The claim specifies that:

-data from an output of a first data processing sub-unit of the multiple data processing sub-units is supplied to the internal state holding circuit before being supplied to an input of a second data processing sub-unit of the multiple data processing sub-units, and

-data from an output of a first data processing unit of the plurality of the data processing units is supplied to the memory portion before being supplied to an input of a second data processing unit of the plurality of the units.

For example, the claimed reconfigurable circuit may correspond to the reconfigurable circuit 12 (FIG. 25), the claimed plurality of data processing units may correspond to circuits FA, FB, FC, FD and FE (FIGS. 28 and 33), the claimed internal state holding circuit may correspond to internal state holding circuit 20 (FIG. 25), the claimed memory portion may correspond to the

memory portion 27 (FIG. 25) and the claimed multiple data processing sub-units may correspond to sub-units such as FA1-FA6, FB1-FB6, FC1-FC6, FD1-FD3 and FE1-FE3 (FIGS. 29-35).

Applicant respectfully submits that the prior art of record does not teach or suggest the claimed processing device arrangement including the reconfigurable circuit with data processing units and sub-units provided in the claimed manner, the internal state holding circuit for receiving data from an output of a first data processing sub-unit before this data is supplied to an input of a second data processing sub-unit, and the memory portion for receiving data from an output of a first data processing unit before this data is supplied to an input of a second data processing unit, as claim 50 requires.

Also, the prior art of record does not teach or suggest first and second data processing sub-units allocated to respectively perform first and second operations, where the second data processing sub-unit is reallocated to perform a third operation when it is not involved in performing the second operation (for example, as illustrated in FIG. 35, a sub-unit of unit FD may be reallocated to perform operation of a sub-unit of unit FE, when it is not involved in performing operation of the unit FD).

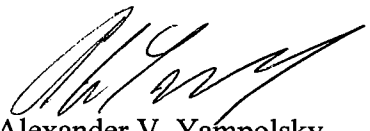
In view of the foregoing, and in summary, claims 50 and 51 are considered to be in condition for allowance.

Favorable reconsideration of the application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Alexander V. Yampolsky
Registration No. 36,324

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 AVY:apr
Facsimile: 202.756.8087
Date: March 31, 2010

Please recognize our Customer No. 20277 as our correspondence address.